IN THE ABSTRACT

Please replace the original abstract with the following abstract:

The design of programmable logic devices, such as FPGAs, may be automated to allow scripts, setup files, and other tool files to be created directly from hollowed and filled netlist, and data-path and design constraint files without extensive human intervention. This allows an FPGA design to be created directly from a logic file to accelerate the FPGA design process. Once hollowed and filled netlists, and data-path and design constraint files have been generated from a design in a standard fashion, the implementation of that design onto an FPGA in an optimized fashion is automated by providing a computer program that is capable of implementing the design, testing the design, evaluating the test results, and altering the design to arrive at a more optimal design. The process may include several steps, such as initial placement of logic groups, sizing of logic groups and FPGA selection, timing analysis, and filled netlist complete design review. The steps may be iterative.